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OH180 PROGRAMMABLE CONTROLLER SOFTWARE: DEVELOPMENT AND INTEGRATION TEST PROCEDURES

Report 87-222-K

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ABSTRACT

This report documents the development and integration test procedures used by the Electrical Research Department during the development of application-independent system software for the OH180 Programmable Controller.

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To Mr. M.A. Machacek
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OH180 PROGRAMMABLE CONTROLLER SOFTWARE:

DEVELOPMENT AND INTEGRATION TEST PROCEDURES

J.D. Bruce

1. INTRODUCTION

This report describes the software test procedures applied by the Electrical Research Department during the development and integration of the OH180 system software, prior to release of the software to Electrical Design Department for systematic functional testing. The procedures apply to newly written software as well as modified versions of previously released software. The report covers the individual detailed testing of separate software submodules, the initial integration testing of the submodules and modules, and finally the overall testing of the integrated modules using special test ladder diagrams. It does not cover the systematic functional testing of the integrated software using actual application ladder diagrams, which the Electrical Design Department conducts after the software is released to them. It also does not include the testing of the application ladder diagrams themselves.

This report forms part of the documentation required for the Software Quality Assurance (SQA) Program for the OH180 as called for in the Darlington SQA Manual/1/. This report was originally circulated in draft form with the number E86-38-K.

The terminology, concepts and conventions are in keeping with those presented in the OH180 Programming Specifications/2/. As indicated in that document, the term "module" is applied to each of the four major components of the OH180 system software:

- OH180 Programmable Controller Executive,
- Programming Station Executive System software,
- Field Monitor software
- Communications Module software.

The term "submodule" refers to an identifiable subsection of a module that has a specified function. It may be a subroutine, a

group of subroutines or a block of in-line coding.

The testing described in this report applies to software that is felt to be correct and ready for release. If "bugs" are known to be present, or are discovered in the course of these tests, appropriate "debugging" or trouble-shooting techniques should be applied to correct the bugs before starting (or restarting) the testing.

2. DETAILED TESTING OF INDIVIDUAL SUBMODULES

The purpose of this level of testing is to demonstrate the correctness of submodules that either have been newly written and are previously untested, or else have been modified since a previous release. The objective is to discover faults which might not emerge (or might emerge in an extremely subtle form) under higher level testing when integrated with other submodules.

When a new software release is being prepared, this level of testing is generally not required for those submodules which have not been changed since the previous release. An exception would be where subsequent testing under Sections 3 and 4 reveals a suspected fault (previously latent) in an unchanged submodule, caused by a change or addition in some other submodule.

The detailed testing of submodules consists of the following steps:

2.1 Visual Inspection

2.1.1 For previously unreleased submodules:

2.1.1.1 Check the submodule for adherence to the requirements of Section 3 of the OH180 Programming Specifications document/2/ (eg appropriate use of comments, appropriate assignment of variable and constants, use of standard entry/exit, etc). Verify that there are no mechanical coding errors detected by the compiler or assembler.

2.1.1.2 Walk through the submodule to check that it apparently implements the required function correctly and that all cases and subcases are handled correctly.

2.1.2 For previously released submodules:

2.1.2.1 By using a source comparison program (eg "SRCOM") or by other means, identify all source code changes since the previous release.

2.1.2.2 Check the source code comments and/or other applicable records for completeness of edit-

ing history. All changes from previous versions are to be recorded.

2.1.2.3 Inspect all coding changes for correct implementation of the functional changes or correction of bugs identified in the problem report (if applicable) and the draft release note. Check that there are no mechanical coding errors detected by the compiler or assembler.

2.1.2.4 Inspect all coding changes for possible unforeseen side effects.

2.2 Operating Tests

2.2.1 By using an in-circuit emulator, logic analyzer, oscilloscope, special test routines or other suitable aids, verify that the submodule, or in some cases each section of the submodule, operates correctly. The details of this procedure are highly dependent on the submodule being tested, but generally involve the following steps:

2.2.1.1 For the section being tested, set up test data to exercise all relevant cases. Make sure extreme value cases are included, such as zero. Also include pathological cases (data out of range, inconsistent or missing) where applicable.

2.2.1.2 By starting execution at the beginning of the section being tested, or by other means, arrange for the section to execute using the desired data.

2.2.1.3 By stopping execution at the end of the section and obtaining a printout, or by other appropriate means, determine that the section handles the test data appropriately.

2.2.2 The following examples illustrate the foregoing procedure:

2.2.2.1 Example 1 - The compiler has been modified to handle "MCR" elements in a different way from the previous release.

Prepare several ladder diagrams containing MCRs used in various possible ways, including cases of an MCR in the first line of the ladder, the last line of the ladder, and not present at all. Compile each ladder and obtain a hex dump of the compiled ladder code. Verify the position and values of the poin-

ters and data tables. Disassemble the relevant section of ladder code to verify that the MCR was correctly handled. Note: Variations of this example were used extensively in the development of the programming station software to verify the capability of the compiler to compile ladder diagrams correctly.

2.2.2.2 Example 2 - The OH180 executive has been modified by adding a new fault testing feature.

Set up an OH180 PC running the new executive and a suitable ladder diagram, under the control of an in-circuit emulator. Set-up the in-circuit emulator to trace the program steps and halt at the end of the new routine that handles the new type of fault. Start the program. Then artificially induce the fault and examine the resulting trace to verify proper operation of the new fault routine.

3. INTEGRATION TESTING

The purpose of this level of testing is to verify, at a functional level, that the submodules and modules work together properly when re-integrated following a modification to a particular submodule (or installation of a new submodule). The emphasis is on testing the capability of the overall integrated software to handle correctly the things that the submodule(s) were written or modified to do (ie the added feature, the modified feature, the elimination of a bug, etc). It is not intended to exercise all aspects of the OH180 system, although in most cases if there are unforeseen side effects of a modification not found in the section 2 tests, they will be uncovered here.

Although the test can be applied following a modification to two or more submodules, it is usually preferable to apply it once after each submodule has been modified, in order to minimize the complexity of subtle fault interactions.

As was the case with the operating tests of Section 2.1, the details of this procedure are highly dependent on the submodule(s) being tested, but the general steps are as follows:

3.1 Devise a ladder diagram that will exercise the added or modified feature, or that will create the conditions which formerly led to the observed bug, as the case may be. Where there is more than one case involved with the feature or bug, devise the ladder diagram to exercise all the cases. Devise more than one ladder diagram if necessary.

3.2 Using the test ladder(s) of the foregoing section, systematically work through the integrated software at the user

level (ie enter, edit, compile, print, program an EPROM, run the OH180 Programmable Controller, connect the Communications Modules, connect the Field Monitor etc), until the conditions are present where the new or modified feature, or absence of the bug, can be functionally tested and verified. At this point thoroughly test the various cases.

3.3 Systematically work through the rest of the integrated software at the user level, up to the point of monitoring and single stepping the ladder(s) using the Field Monitor, and setting up the Communications Module loop if applicable, in order to look for unforeseen side effects.

4. OVERALL FUNCTIONAL TESTING

The purpose of this level of testing is to provide an overall functional verification of the complete integrated OH180 system software. It broadly covers all aspects of the system software, and is intended as a final pre-release check-out test, to detect any residual cases of faults in one submodule being triggered by a recent modification to another. However, it does not test any one aspect to great depth and it does not take the place of the comprehensive functional testing of the integrated software carried out by the Electrical Design Department after the software is released to them.

In general, the overall functional testing consists of carrying out all of the following steps. In certain cases some of the steps may not be applicable; for example if a new version of the Communications Module executive is being released but the rest of the system is unchanged, then clearly steps 4.1 and 4.2 would be pointless. Also, for some preliminary software releases, some of the steps may be judged unnecessary. Normally, however, all steps are applicable.

4.1 SYST1 and SYSTEX Tests

4.1.1 Program a pair of EPROM modules with the SYST1 and SYSTEX ladder diagrams described in Section 8.6 of the OH180 PC Manual/3/.

4.1.2 Using a fully configured OH180 crate, carry out the test procedure PC-TP-SYST given in Appendix D.6 of the PC Manual.

4.1.3 During the time that each of SYST1 and SYSTEX are running, plug in a Field Monitor (or Test Monitor if no Field Monitor is available) and verify the correct disassembly and display of the operating ladder. Verify that the fault conditions generated as part of the SYST procedure are correctly shown on the monitor.

4.2 FUNC and FUNCEX Tests

FUNC and FUNCEX are complex ladder diagrams designed to test the dynamic operation of all I/O points on an OH180 Programmable Controller.

Note: Although this section is written for both the FUNC and FUNCEX tests to be applied, it is normally fully sufficient from a software testing viewpoint, to apply only one of the two (usually FUNCEX).

4.2.1 Program EPROM modules with the FUNC and FUNCEX test programs described in Section 8.7 of the OH180 PC Manual/3/.

4.2.2 Using a fully configured half crate, carry out the test procedure PC-TP-FUNC given in Appendix D.7 of the OH180 PC Manual/3/. Repeat the procedure with a fully expanded crate using FUNCEX.

4.2.3 During the time that each of FUNC and FUNCEX are running, plug in a Field Monitor (or Test Monitor if no Field Monitor is available) and verify the correct disassembly and display of the operating ladder.

4.3 Communications Module GO/NOGO Test

This test exercises all aspects of the Communications Module (CM) executive.

Note: This test only needs to be done if the Communications Module executive has been modified.

4.3.1 The procedure for this test is given in document CM-TP-GONOGO, in Appendix D of the Communications Module Technical Manual/4/.

4.4 SIMTST

SIMTST is a relatively simple ladder diagram incorporating all OH180-supported ladder elements except communications points. A listing of SIMTST is given in Figure 1.

4.4.1 Manually enter the SIMTST ladder using the ladder entry software.

4.4.2 Save and restore the ladder file.

4.4.3 Print the ladder. Verify the correctness of the printout.

4.4.4 Compile and program the ladder onto an EPROM Module.

4.4.5 Load and run in a suitably configured OH180 PC, suitably wired with input switches for points 1-12 of slot 1 and lamps for output points 1-8 of slot 2. By manipulating the switches and observing the lamps, verify that all elements in the ladder operate correctly.

4.4.6 Use the Test Monitor to download the SIMTST binary file to the OH180 (using a Power Supply - RAM module in place of the regular PCD1 Power Supply).

4.4.7 Plug in a freshly powered up Field Monitor (or Test Monitor if no Field Monitor is available) and verify the correct disassembly and display of the operating ladder. Verify that both or all forcing modes operate correctly for all element types. Verify that forces work when and only when the force key is in the enable position. Obtain a ladder print out and verify its correctness.

4.5 COMTST-A and COMTST-B

COMTST-A and COMTST-B are a pair of simple ladder diagrams designed to exercise the communications capability of the OH180 System Software. They require two OH180 PCs and two Communications Modules arranged in a two-station dual ring fiber optic loop. This test is designed to check out the various interactions among the PCs and the CMs. By extending the concept to COMTST-C and COMTST-D etc, loops of any size up to 32 can be set up. For most testing, however, two are sufficient.

Listings of COMTST-A and COMTST-B are given in Figure 2.

4.5.1 Enter, compile, program and run the ladders COMTST-A and COMTST-B on two suitably configured OH180 PCs, connected through CMs as a two-station dual ring loop. Verify that the system runs properly, without errors. Verify that each PC exhibits a characteristic flashing of its slot 2 point 2 LED: one at about three cycles per two seconds and the other at about three cycles per four seconds.

4.5.2 Plug a Field Monitor (or Test Monitor if no Field Monitor is available) into one of the CPUs and verify the correct disassembly and display of the operating ladder. Verify that both forcing modes (ON or OFF) operate correctly for all elements on the ladder.

4.5.3 Introduce the following errors and verify that the loop responds correctly and the appropriate errors are displayed on all relevant LEDs as well as on the Field Monitor:

4.5.3.1 Remove a fiber optic connector.

4.5.3.2 Remove an RS232 connector (on the PC not monitored by the Field Monitor).

4.5.3.3 Power down the corresponding CM.

4.5.3.4 Restore the foregoing items and press the ACKNOWLEDGE buttons as required.

5. RELEASE AND DOCUMENTATION

5.1 Release Criteria

If all aspects of the system software pass their various tests in Sections 2,3 and 4, and no errors or malfunctions are detected (except as specifically provided for, as part of the test), and if the software designers and reviewers are satisfied that the tests conducted under Section 2 are sufficient in view of the extent of the new or revised coding, then the software is ready for release to the Electrical Design Department for detailed functional testing of the integrated system software. If any failures occur in the tests of Sections 2,3 or 4, the software cannot be released until the reason for the failure is identified and, if necessary, the software corrected and retested. (In some cases it my be desirable to release the software notwithstanding a known "bug". In such cases the nature and extent of the bug must be clearly identified in the release notes.)

5.2 Documentation

5.2.1 All software releases are to be provided with release notes, in keeping with the requirements set down in Section 5 of the OH180 Programming Specifications document/2/.

5.2.2 For all software releases to Electrical Design up to June 1986, formal documentation of the development testing (as outlined in the present report) was not required. The release notes themselves provide an implicit assertion that the appropriate testing was carried out, although they do not provide the details. For example, when the release notes state that a particular bug was fixed, one can infer that individual and integration tests (ie Section 2 and Section 3) were carried out. For certain releases, some of the Overall Functional Tests (Section 4) were judged unnecessary in view of the limited nature of the software changes being released, and were omitted. These were carried

out, however, when there was any reasonable possibility of a fault being detected by them.

5.2.3 For any OH180 system software releases subsequent to June 1986, formal documentation is required for the testing covered by the present report. The reason for this is that the June 1986 release has been subjected to extensive formal testing by the Electrical Design Department and was used to prepare ladder diagrams issued to Darlington NGS. Subsequent releases will therefore require rigorous and well documented scrutiny to ensure that the prior testing and field experience is still applicable.

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REFERENCES

1. Software Quality Assurance (SQA) Manual for Ontario Hydro's OH180 Programmable Controller: Darlington GS; Electrical Design Department, November 27, 1986.

2. Bruce, J.D., "Programming Specifications for the OH180 Programmable Controller Software", Electrical Research Report 87-221-K.

3. Griffin, J.D.A., "OH180 Programmable Controller Manual", Research Report 84-281-H, October 29, 1984.

4. Whitmell, H.E., "OH180 Communications Module Technical Manual", Research Report 85-255-H.

TEST PROGRAM SIMTST IO------

TEST PROCEDURE FOR SIMTST:

1. MANUALLY ENTER THE LADDER DIAGRAM STARTING AT THE LINE OF TEXT CONTAINING 'TEXT - LINE 1'. DO NOT ENTER THIS TEST PROCEDURE. IT IS INCLUDED HERE FOR DOCUMENTATION ONLY.

2. SAVE, PRINT, COMPILE AND PROGRAM THE LADDER INTO AN EPROM MODULE.

3. SET UP AN UNEXPANDED OH180 WITH I/O CONFIGURATION IO--.

4. CONNECT 11 ON/OFF SWITCHES TO SLOT 1, POINTS 1-11.

5. CONNECT 6 LAMPS TO SLOT 2 POINTS 1-6.

6. SET THE SWITCHES AS SHOWN IN THE TABLE BELOW AND VERIFY THAT THE LAMPS OPERATE AS INDICATED.

SWITCH	LAMPS (- = OFF, 1 = ON, F = FLASHING) #1	#2	#3	#4	#5	#6
ALL OFF	1	-	-	-	-	F
4 ON	-	-	-	-	-	F
2 ON	1	-	-	-	-	F
4 OFF	1	-	-	-	-	F
4 ON	1	-	-	-	-	F
1 ON	-	-	-	-	-	-
2 OFF	-	-	-	-	-	-
1 OFF	-	-	-	-	-	F
3 ON	-	-	-	-	-	F
2 ON	-	-	-	-	-	F
3 OFF	1	-	-	-	-	F
2 OFF	-	-	-	-	-	F
3 ON	-	-	-	-	-	F
6 ON	-	1	-	-	-	F
5 ON	-	1	-	-	-	F
6 OFF	-	1	-	-	-	F
5 OFF	-	-	-	-	-	F
5 ON	-	-	-	-	-	F
7 ON	-	-	-	-	-	F
THEN AFTER 10 SEC:	-	-	1	-	-	F
7 OFF	-	-	-	-	-	F
7 ON FOR 5 SEC, THEN OFF	-	-	-	-	-	F
9 ON	-	-	-	-	-	F
8 ON FOR 10 SEC	-	-	-	-	-	F
9 OFF	-	-	-	-	-	F
THEN AFTER 5 SEC:	-	-	-	1	-	F
8 OFF	-	-	-	1	-	F
9 ON	-	-	-	-	-	F
9 OFF	-	-	-	-	-	F
8 ON FOR 2 SEC, THEN OFF	-	-	-	-	-	F
10 ON AND OFF 4 TIMES	-	-	-	-	-	F
10 ON	-	-	-	-	1	F
10 OFF	-	-	-	-	1	F
10 ON AND OFF 5 TIMES	-	-	-	-	1	F
11 ON	-	-	-	-	-	F
10 ON AND OFF 10 TIMES	-	-	-	-	-	F
11 OFF	-	-	-	-	-	F
10 ON AND OFF 4 TIMES	-	-	-	-	-	F
10 ON	-	-	-	-	1	F

7. THE TEST PROCEDURE IS COMPLETE WHEN ALL LAMPS OPERATE AS INDICATED IN THE ABOVE TABLE.

BEGIN ENTERING THE LADDER DIAGRAM AT THE FOLLOWING LINE OF TEXT

TEXT - LINE 1

Figure 1: Test Ladder "SIMTST" (Reference: Section 4.4)

TEST PROGRAM SIMTST IO------

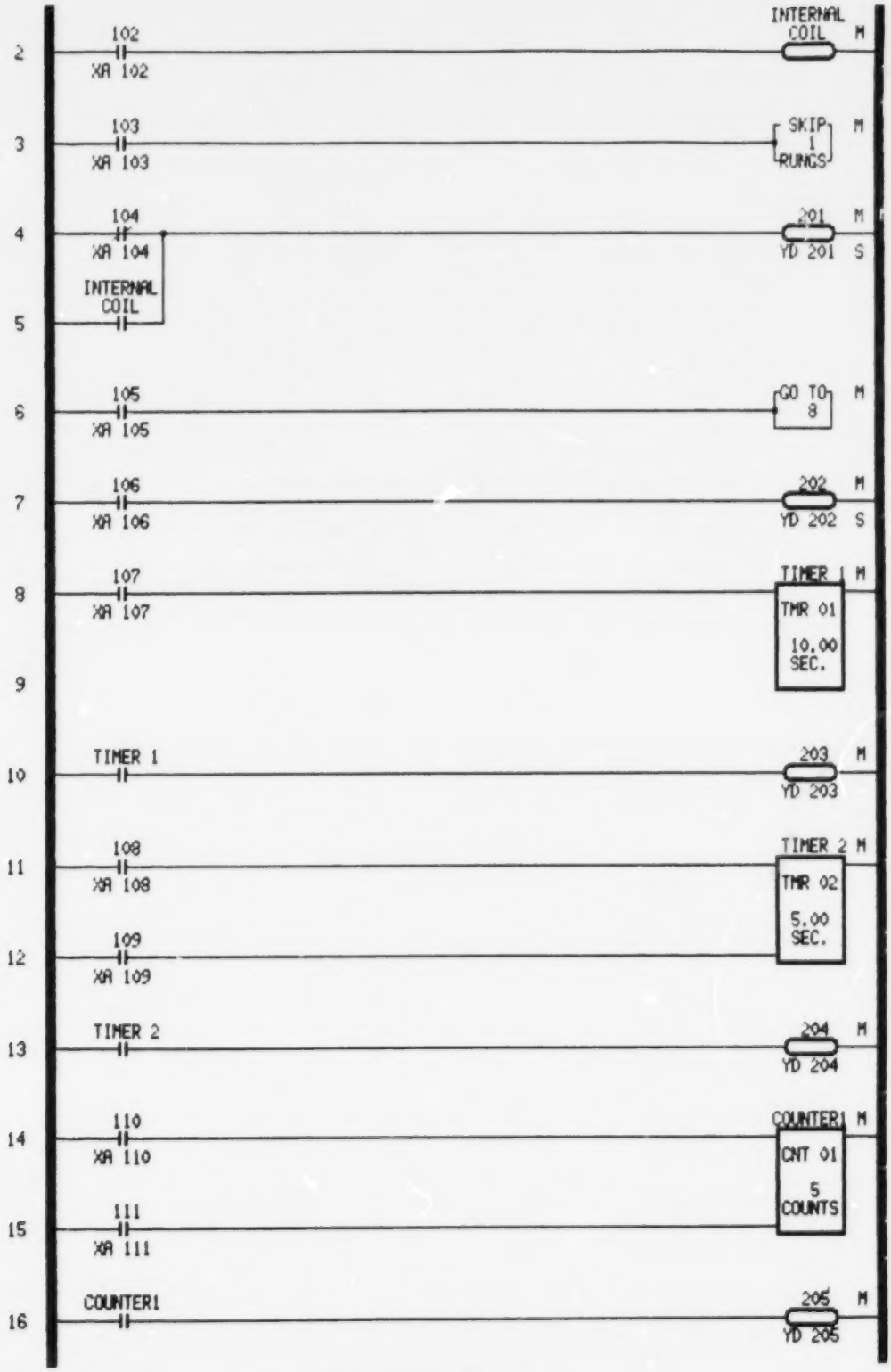

Figure 1: Test Ladder "SIMTST" (Reference: Section 4.4)

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TEST PROGRAM SIMTST IO------

Figure 1: Test Ladder "SIMTST"
(Reference: Section 4.4)

LABEL CROSS-REFERENCE TABLE

TEST PROGRAM SIMTST IO------

System ID: 100-00000-PK4095
File: PK4095.W06
Date Created: 09-DEC-86 13:12:52
Designer: J. BRUCE
Switch Settings: 111111111111
Card usage: IO-- ----

EXTERNAL LABELS

Slot: 1 Type: Input

I/O no.		Label	References
XA101	101		1
XA102	102		2
XA103	103		3
XA104	104		4
XA105	105		6
XA106	106		7
XA107	107		8
XA108	108		11
XA109	109		12
XA110	110		14
XA111	111		15
XA112			
XA113			
XA114			
XA115			
XA116			
XA117			
XA118			
XA119			
XA120			
XA121			
XA122			
XA123			
XA124			

Figure 1: Test Ladder "SIMTST"
(Referebce: Section 4.4)

Slot: 2 Type: Output

I/O no.	Label	References
YD201	201	4*
YD202	202	7*
YD203	203	10*
YD204	204	13*
YD205	205	16*
YD206	206	17*
YD207		
YD208		
YC209		
YC210		
YC211		
YC212		
YC213		
YC214		
YC215		
YC216		

("*" = Controlled device)

(NO COMMUNICATION OUTPUTS USED)

(NO COMMUNICATION INPUTS USED)

Figure 1: Test Ladder "SIMTST" (Reference: Section 4.4)

INTERNAL STATUS FLAGS

Label		References
COMM.	FLAG 1	
COMM.	FLAG 2	
COMM.	FLAG 3	
COMM.	FLAG 4	
COMM.	FLAG 5	
COMM.	FLAG 6	
COMM.	FLAG 7	
COMM.	FLAG 8	
MULTIPLE	GRND FLT	
WIRING	FAULT	
I/O CARD	FAULT	
CPU CARD	FAULT	
SYSTEM	GRND FLT	
WATCHDOG	TIME-OUT	
SYSTEM	RESTART	
ALL	OKAY	
REMOTE	COMM ACK	
PK/SYS	FAULT	
FATAL	I/O FLT	
FLASHER	RESET	
FAST	FLASHER	
SLOW	FLASHER	17
TEMP SYS	GRND FLT	
ACK		

("*" = Controlled device)

INTERNAL LABELS

Tmr/Cnt	Label	References
CNT 1	COUNTER1	14* 16
	INTERNAL COIL	2* 5
TMR 1	TIMER 1	8* 10
TMR 2	TIMER 2	11* 13

("*" = Controlled device)

Figure 1: Test Ladder "SIMTST"
(Reference: Section 4.4)

TIMER SETTINGS

No.	Label	Setting	No.	Label	Setting
1	TIMER 1	10.00	2	TIMER 2	5.00
3			4		
5			6		
7			8		
9			10		
11			12		
13			14		
15			16		
17			18		
19			20		
21			22		
23			24		

COUNTER SETTINGS

No.	Label	Setting	No.	Label	Setting
1	COUNTER1	5	2		
3			4		
5			6		
7			8		
9			10		
11			12		
13			14		
15			16		
17			18		
19			20		
21			22		
23			24		

Figure 1: Test Ladder "SIMTST"
(Reference: Section 4.4)

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PRINTOUT: W03 100-00000-PK0001 0H180 06-NOV-86 16:14 PAGE 1

COMMUNICATION TEST PROGRAM COMTST-A --O-----

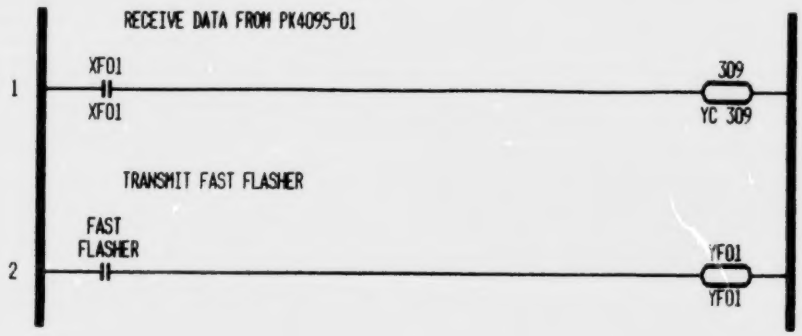

Figure 2: Communication Test Ladders "COMTST-A" and "COMTST-B"
(Reference: Section 4.5)

Page 1 of 6

LABEL CROSS-REFERENCE TABLE

COMMUNICATION TEST PROGRAM COMTST-A --O-----

System ID: 100-00000-PK0001
File: PK0001.W03
Date Created: 06-NOV-86 16:12:16
Designer: OH180
Switch Settings: 000000000001
Card usage: --O- ----

EXTERNAL LABELS

Slot: 3 Type: Output

I/O no.	Label	References
YD301		
YD302		
YD303		
YD304		
YD305		
YD306		
YD307		
YD308		
YC309	309	1*
YC310		
YC311		
YC312		
YC313		
YC314		
YC315		
YC316		

("*" = Controlled device)

COMMUNICATION OUTPUT LABELS

I/O no.	Label	References
YF01	YF01	2*

("*" = Controlled device)

COMMUNICATION INPUT LABELS

I/O no.	Sending PC	Label	References
XF01	PK4095-01	XF01	1

Figure 2: Communication Test Ladders "COMTST-A" and "COMTST-B"
(Reference: Section 4.5)

INTERNAL STATUS FLAGS

Label	References
COMM. FLAG 1	
COMM. FLAG 2	
COMM. FLAG 3	
COMM. FLAG 4	
COMM. FLAG 5	
COMM. FLAG 6	
COMM. FLAG 7	
COMM. FLAG 8	
MULTIPLE GRND FLT	
WIRING FAULT	
I/O CARD FAULT	
CPU CARD FAULT	
SYSTEM GRND FLT	
WATCHDOG TIME-OUT	
SYSTEM RESTART	
ALL OKAY	
REMOTE COMM ACK	
PK/SYS FAULT	
FATAL I/O FLT	
FLASHER RESET	
FAST FLASHER	2
SLOW FLASHER	
TEMP SYS GRND FLT	
ACK	

("*" = Controlled device)

(NO INTERNAL LABELS USED)

(NO TIMERS USED)

(NO COUNTERS USED)

Figure 2: Communication Test Ladder "COMTST-A" and "COMTST-B"
(Reference: Section 4.5)

PRINTOUT: W03 100-00000-PK4095 0H180 06-NOV-86 16:18 PAGE 1

COMMUNICATION TEST PROGRAM COMTST-B --O-----

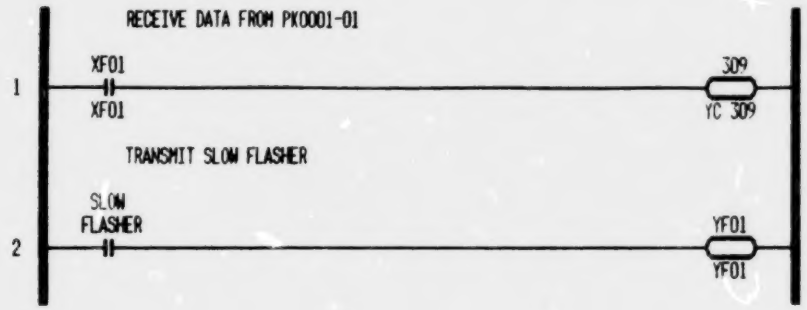

Figure 2: Communication Test Ladders "COMTST-A" and "COMTST-B"
(Reference: Section 4.5)

LABEL CROSS-REFERENCE TABLE

COMMUNICATION TEST PROGRAM COMTST-B --O-----

System ID: 100-00000-PK4095
File: PK4095.W03
Date Created: 06-NOV-86 16:16:12
Designer: OH180
Switch Settings: 111111111111
Card usage: --O- ----

EXTERNAL LABELS

Slot: 3 Type: Output

I/O no.	Label	References
YD301		
YD302		
YD303		
YD304		
YD305		
YD306		
YD307		
YD308		
YC309	309	1*
YC310		
YC311		
YC312		
YC313		
YC314		
YC315		
YC316		

("*" = Controlled device)

COMMUNICATION OUTPUT LABELS

I/O no.	Label	References
YF01	YF01	2*

("*" = Controlled device)

COMMUNICATION INPUT LABELS

I/O no.	Sending PC	Label	References
XF01	PK0001-01	XF01	1

Figure 2: Communication Test Ladders "COMTST-A" and "COMTST-B"
(Reference: Section 4.5)

INTERNAL STATUS FLAGS

Label		References
COMM.	FLAG 1	
COMM.	FLAG 2	
COMM.	FLAG 3	
COMM.	FLAG 4	
COMM.	FLAG 5	
COMM.	FLAG 6	
COMM.	FLAG 7	
COMM.	FLAG 8	
MULTIPLE	GRND FLT	
WIRING	FAULT	
I/O CARD	FAULT	
CPU CARD	FAULT	
SYSTEM	GRND FLT	
WATCHDOG	TIME-OUT	
SYSTEM	RESTART	
ALL	OKAY	
REMOTE	COMM ACK	
PK/SYS	FAULT	
FATAL	I/O FLT	
FLASHER	RESET	
FAST	FLASHER	
SLOW	FLASHER	2
TEMP SYS	GRND FLT	
ACK		

("*" = Controlled device)

(NO INTERNAL LABELS USED)

(NO TIMERS USED)

(NO COUNTERS USED)

Figure 2: Communication Test Ladders "COMTST-A" and "COMTST-B"
(Reference: Section 4.5)